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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/935,894	08/23/2001	Geoffrey F. Burns	US 010412	1354

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	4

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/935,894	BURNS ET AL.
	Examiner	Art Unit
	Dipakkumar Gandhi	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 August 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3, 01/03/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because in figures 1, 3, 4, 5, 6, 8, 9 and 10, the labels for the items have only numbers. The items should have descriptive labels. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 10 is objected to because of the following informalities: On page 17, line 2 of claim 10, "error identification mean" is incorrect. It should be --error identification means--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Wolf (US 6,385,751 B1).

Wolf anticipates claim 16.

Wolf teaches a method for selecting a unique set of electronic decoder elements from a plurality of decoder elements in an integrated circuit (IC) to implement one Reed-Solomon Decoder from a plurality of possible Reed-Solomon (R-S) decoders (figure 6, abstract, col. 6, lines 37-44, Wolf),

comprising the steps of: a) loading a Galois field symbol size parameter into

the IC (col. 23, lines 25-29, Wolf); b) loading a plurality of multiplier coefficients into the IC (col. 18, lines 5-9, Wolf).; c) loading a data block size parameter n into the IC (col. 23, lines 53-55, Wolf); and d) loading a parity symbol width size parameter into the IC (col. 19, line 39, Wolf).

- Wolf anticipates claim 17.

Wolf teaches a method wherein the Galois field symbol size parameter comprises 7 or 8 bits (col. 19, line 39, Wolf).

- Wolf anticipates claim 18.

Wolf teaches a method wherein the plurality of multiplier coefficients are characterized in that a particular R-S polynomial is implemented in the IC (abstract, col. 18, lines 5-9, Wolf).

- Wolf anticipates claim 19.

Wolf teaches a method for correcting data errors in a serial data block using an integrated circuit (IC) having a configurable Reed-Solomon (R-S) error-correction decoder (figure 6, abstract, col. 6, lines 37-39, col. 15, lines 21-23, Wolf), comprising the steps of: a) loading a plurality of configuration parameters into the IC (col. 18, lines 5-9, Wolf); b) inputting a first data block into the IC (col. 23, lines 25-26, Wolf); c) processing the data block in the configured IC to identify and enumerate any data errors in the data block d) outputting a corrected data block if the number of errors are below a predetermined threshold; or e) outputting an error signal if the number or errors exceeds the predetermined threshold (col. 15, lines 21-52, Wolf).

- Wolf anticipates claim 20.

Wolf teaches a method wherein the data block comprises a portion relating to data and a portion relating to parity checking (col. 2, lines 52-55, Wolf).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolf (US 6,385,751 B1) in view of Hocevar et al. (US 6,256,724 B1).

As per claim 1, Wolf teaches a universal Reed-Solomon (R-S) decoding integrated circuit (IC) for correcting errors in a received data bit stream signal having a selectable data width and a selectable data block size (figure 6, 10C, abstract, col. 6, lines 37-39, col. 12, lines 27-35, col. 15, lines 21-23, Wolf), comprising:

A configuration control means (figure 6, 9, col. 6, lines 37-44, col. 11, lines 10-11, Wolf);

A data input means (col. 24, lines 60-61, Wolf);

A plurality of arithmetic-operation blocks (col. 24, lines 37-39, Wolf);

and an error identification means (figure 7, col. 15, lines 48-52, Wolf);

an error correction means and a data output means (col. 15, lines 21-23, Wolf).

However Wolf does not explicitly teach the specific use of a configurable computational processing means, further comprising: a plurality of configurable arithmetic-operation blocks; a plurality of configurable interconnections between the configurable arithmetic-operation blocks.

Hocevar et al. in an analogous art teach that the co-processor is responsive to the commands to configure itself correspondingly whereby the co-processor is operable to perform a set of related data processing operation (col. 17, lines 12-15, Hocevar et al.)

Hocevar et al teach that fig. 5 illustrates another possible arrangement of circuit 100. Circuit

100 illustrated in FIG. 5 includes two reconfigurable hardware co-processors. Digital signal processor core 110 operates with first reconfigurable hardware co-processor 140 and second reconfigurable hardware co-processor 180 (col. 11, lines 9-14, Hocevar et al.). Hocevar et al teach that figs. 6 to 9 illustrate the construction of an exemplary reconfigurable hardware co-processor. Fig. 6 illustrates the overall general architecture of multiple multiply-accumulator 140. Datapath 170 is the operational portion of the co-processor. Datapath 170 includes plural hardware multipliers and adders that are connectable in various ways to perform a variety of multiply-accumulate operations. The operations of co-processor 140 are under control of control unit 190. Control unit 190 recalled the commands from command memory 141 and provides the corresponding control within co-processor 140 (figures 6-9, col. 11, lines 31-32, lines 37-38, lines 52-56, lines 64-67, Hocevar et al.). Hocevar et al teach that fig. 8 illustrates in block diagram form the construction of datapath 170. Multiplexer 317 selects from among three quantities. The first quantity is a concatenation of the 16 Data X bits and 16 Data Y bits at the input. This input allows multiplier 312 to be bypassed. The second quantity is the product supplied by multiplier 312. The third quantity is the shifted output of 8 bit right shifter 315 (figure 8, col. 12, lines 25-26, lines 54-57, lines 60-62, Hocevar et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolf's patent with the teachings of Hocevar et al. by including an additional step of using a configurable computational processing means, further comprising: a plurality of configurable arithmetic-operation blocks; a plurality of configurable interconnections between the configurable arithmetic-operation blocks.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to configure the arithmetic operation blocks and interconnection between them based on the different size and symbol width of the data blocks and the processing requirements for efficient decoding of the data received.

- As per claim 2, Wolf and Hocevar et al. teach the additional limitations.

Wolf teaches the universal R-S decoding IC, wherein the configuration control means comprises a plurality of user input parameters (col. 18, lines 5-9, Wolf).

- As per claim 3, Wolf and Hocevar et al. teach the additional limitations.

Wolf teaches the universal R-S decoding IC, wherein the configuration control means comprises a means for implementing one data width configuration from a plurality of data width configurations (figure 10c, col. 12, lines 27-35, Wolf).

- As per claim 4, Wolf and Hocevar et al. teach the additional limitations.

Wolf teaches the universal R-S decoding IC, wherein the configuration control means comprises a means for implementing one data block size from a plurality of data block sizes (abstract, Wolf).

- As per claim 5, Wolf and Hocevar et al. teach the additional limitations.

Wolf teaches that he universal R-S decoding IC, wherein the configuration control means comprises a means for inputting scalar coefficients (col. 18, lines 5-9, Wolf).

- As per claim 6, Wolf and Hocevar et al. teach the additional limitations.

Hocevar et al. teach the universal R-S decoding IC, wherein each one of the plurality of configurable arithmetic-operation blocks further comprises a plurality of logical circuit gates needed to implement one or more of the mathematical operations from the group consisting of addition, multiplication, and inversion (figures 1, 6 to 9, col. 3, lines 41-43, col. 11, lines 31-32, lines 52-56, Hocevar et al.). Wolf teaches logic circuit gates (figures 2, 5, col. 5, lines 38, 64-65, Wolf).

- As per claim 7, Wolf and Hocevar et al. teach the additional limitations.

Hocevar et al. teach a plurality of configurable arithmetic-operation blocks has a computation means (figures 5-9, col. 11, lines 9-11, lines 31-35, Hocevar et al.). Wolf teaches a configuration control receiving means (figure 6, 9, col. 6, lines 37-44, col. 11, lines 10-11, Wolf); a data signal input means (col. 24, lines 60-61, Wolf); an error-correction means and a data signal output means (col. 15, lines 21-23, Wolf).

- As per claim 8, Wolf and Hocevar et al. teach the additional limitations.

Wolf teaches the universal R-S decoding IC, wherein the configurable computational processing means is configured by the loading of one or more coefficients from the configuration control means (figure 9, col. 11, lines 41-48, Wolf).

- As per claim 9, Wolf and Hocevar et al. teach the additional limitations.

Wolf teaches the universal R-S decoding IC, wherein the configurable computational processing means is characterized in that hardware for a first Galois field can perform mathematical operations on a second Galois field (col. 23, lines 45-50, Wolf).

- As per claim 10, Wolf and Hocevar et al. teach the additional limitations.

Wolf teaches the universal R-S decoding IC, wherein the error identification means computes the error location and magnitude in an inputted data block (col. 15, lines 21-30, Wolf).

8. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolf (US 6,385,751 B1) in view of Kroun et al. (US 6,584,560 B1).

As per claim 11, Wolf teaches an integrated circuit (IC) for correcting data errors using a Reed-Solomon (R-S) decoder (figure 6, col. 6, lines 37-39, col. 15, lines 21-23, Wolf), comprising a configuration control means (figure 6, 9, col. 6, lines 37-44, col. 11, lines 10-11, Wolf).

However Wolf does not explicitly teach the specific use of a first selectable computational processor and a second selectable computational processor and for selecting one and only one of the computational processors.

Kroun et al. in an analogous art teach that the computer system includes a plurality of computer processors. The initialization control circuit includes a memory having data identifying one of the processors. The initialization control circuits directs the system to employ the processor identified in the memory as the chief initialization processor (col. 2, lines 56-57, lines 62-64, line 67, col. 3, lines 1-3, Kroun et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolf's patent with the teachings of Kroun et al. by including an additional step of using a first selectable computational processor and a second selectable computational processor and for selecting one and only one of the computational processors.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity

to select a computational processor for efficient decoding based on the parameters of the Galois Field order and the number of symbols for each codeword of the transmitted data.

- As per claim 12, Wolf and Kroun et al. teach the additional limitations.

Wolf teaches a data signal input means (col. 24, lines 60-61, Wolf); an error-correction means, and a data signal output means (col. 15, lines 21-23, Wolf). Kroun et al. teaches the first and the second computational processors each comprise, a computation means (col. 2, lines 56-57, Kroun et al.)

- As per claim 13, Wolf and Kroun et al. teach the additional limitations.

Wolf teaches Reed-Solomon decoder for a data signal having a first width and a data signal having second width (abstract, figure 10c, col. 12, lines 27-35, Wolf). Kroun et al. teach the first computational processor and the second computational processor having a plurality of mathematical functions (col. 2, lines 56-57, Kroun et al.).

- As per claim 14, Wolf and Kroun et al. teach the additional limitations.

Wolf teaches the IC, wherein the first width comprises 8 bits and the second width comprises 7 bits (col. 19, line 39, Wolf).

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolf (US 6,385,751 B1) and Kroun et al. (US 6,584,560 B1) as applied to claim 11 above, and further in view of Hocevar et al. (US 6,256,724 B1).

As per claim 15, Wolf and Kroun et al. substantially teach the claimed invention described in claim 11 (as rejected above). Wolf also teaches a user command input means (col. 18, lines 5-9, Wolf), the Reed-Solomon decoder (abstract, Wolf), and an outputting means for configuring the IC (figure 6, 9, col. 11, lines 41-48, Wolf).

However Wolf does not explicitly teach the specific use of a first selection means for logically selecting one or more arithmetic functional blocks from a plurality of arithmetic functional blocks.

Hocevar et al. teaches that datapath 170 includes a plural hardware multipliers and adders that are connectable in various ways to perform a variety of multiply-accumulate operations (figure 6, col. 11, lines 53-56, Hocevar et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolf's patent with the teachings of Hocevar et al. by including an additional step of using a first selection means for logically selecting one or more arithmetic functional blocks from a plurality of arithmetic functional blocks.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to select the desired arithmetic circuits for decoding data based on the on the parameters of the Galois Field order and the number of symbols for each codeword of the transmitted data.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

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